Amendments to the Claims

1. (Previously presented) A method of chopping an input signal by a chopping amplifier, comprising:

segmenting, by a chopping amplifier, a chopping operation of an input signal across at least two chopping amplifier stages, wherein the at least two chopping amplifier stages are responsive to a master controller and wherein each of the at least two chopping amplifier stages contributes a partial gain amount to an overall gain of the chopping amplifier and wherein the overall gain is a sum of the partial gain amounts of the at least two chopping amplifier stages.

2. (Original) The method according to Claim 1, further comprising:

controlling, by the master controller, operations of the at least two chopping amplifier stages.

3. (Original) The method according to Claim 2, wherein each of the at least two chopping amplifier stages is independently controlled by the master controller.

4. (Original) The method according to Claim 3, wherein the each of the at least two chopping amplifier stages is able to perform its own independent chopping operation.

5. (Original) The method according to Claim 1, further comprising:

staggering chop clock signals of the at least two chopping amplifier stages so that the chop clock signals of the at least two chopping amplifier stages have non-overlapping periods and at least one of the at least two chopping amplifier stages is not operating in an open loop at any given time.

6. (Previously presented) The method according to Claim 5, wherein the non-overlapping periods are periodic non-overlapping periods so that a master chop clock of the master controller can be operated at a lower chop clock frequency and low-level aliasing due to chopping is avoided.

7. (Original) The method according to Claim 1, wherein the at least two chopping amplifier stages are an N number of chopping amplifier stages, wherein N is an integer equal to or greater than two and wherein each of the N number of chopping amplifier stages contributes 1/N amount of an overall gain of the chopping amplifier.

8. (Original) The method according to Claim 7, wherein, for every doubling of N number of chopping amplifier stages, magnitudes of chopping artifacts are reduced by 3 dB.

9. (Original) The method according to Claim 7, wherein, for every doubling of N number of chopping amplifier stages, aliased components are reduced by 3 dB.

10. (Original) The method according to Claim 1, wherein the at least two chopping amplifier stages are coupled together in parallel.

11. (Previously presented) A chopping amplifier for chopping an input signal, comprising:

at least two chopping amplifier stages, wherein a chopping operation of an input signal is segmented across the at least two chopping amplifier stages and wherein the at least two chopping amplifier stages are responsive to a master controller and wherein each of the at least two chopping amplifier stages contributes a partial gain amount to an overall gain of the chopping amplifier and wherein the overall gain is a sum of the partial gain amounts of the at least two chopping amplifier stages.

12. (Original) The chopping amplifier according to Claim 11, further comprising:

a master controller for controlling operations of the at least two chopping amplifier stages.

13. (Original) The chopping amplifier according to Claim 12, wherein the master controller independently controls each of the at least two chopping amplifier stages.

14. (Original) The chopping amplifier according to Claim 13, wherein the each of the at least two chopping amplifier stages is able to perform its own independent chopping operation.

15. (Original) The chopping amplifier according to Claim 11, wherein chop clock signals of the at least two chopping amplifier stages are staggered so that the chop clock signals of the at least two chopping amplifier stages have non-overlapping periods and at least one of the at least two chopping amplifier stages is not operating in an open loop at any given time.

16. (Previously presented) The chopping amplifier according to Claim 15, wherein the non-overlapping periods are periodic non-overlapping periods so that a master chop clock of the master controller can be operated at a lower chop clock frequency and low-level aliasing due to chopping is avoided.

17. (Original) The chopping amplifier according to Claim 11, wherein the at least two chopping amplifier stages are an N number of chopping amplifier stages, wherein N is an integer equal to or greater than two and wherein each of the N number of chopping amplifier stages contributes 1/N amount of an overall gain of the chopping amplifier.

18. (Original) The chopping amplifier according to Claim 17, for every doubling of N number of chopping amplifier stages, magnitudes of chopping artifacts are reduced by 3 dB.

19. (Original) The chopping amplifier according to Claim 17, for every doubling of N number of chopping amplifier stages, aliased components are reduced by 3 dB.

20. (Original) The chopping amplifier according to Claim 11, wherein the at least two chopping amplifier stages are coupled together in parallel.

21. (Previously presented) The chopping amplifier according to Claim 17, wherein the non-overlapping periods are periodic non-overlapping periods so that a master chop clock of the master controller can be operated at a lower chop clock frequency fc and low-level aliasing due to chopping is avoided wherein the lower chop clock frequency fc is set equal to a sampling frequency fs / (2 * N).

22. (Previously presented) The chopping amplifier according to Claim 11, wherein:

during non-switch transition periods, all of the at least two chopping amplifier stages are active and chopping; and

during a switch transition period, one of the at least two chopping amplifier stages is disconnected while all remaining ones of the at least two chopping amplifier stages are chopping.

23. (Previously presented) The method according to Claim 7, wherein the non-overlapping periods are periodic non-overlapping periods so that a master chop clock of the master controller can be operated at a lower chop clock frequency fc and low-level aliasing due to chopping is avoided wherein the lower chop clock frequency fc is set equal to a sampling frequency fs / (2 * N).

24. (Previously presented) The method according to Claim 1, wherein:

during non-switch transition periods, all of the at least two chopping amplifier stages are active and chopping; and

during a switch transition period, one of the at least two chopping amplifier stages is disconnected while all remaining ones of the at least two chopping amplifier stages are chopping.